

PRELIMINARY AMENDMENT

Serial Number: 08/902,133

Filing Date: July 29, 1997

Title: DYNAMIC ELECTRICALLY ALTERABLE PROGRAMMABLE READ ONLY MEMORY DEVICE

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wherein the intergate dielectric has a permittivity that is higher than a permittivity of silicon dioxide.

32.(Amended)

A memory device comprising:

a plurality of memory cells, wherein each memory cell includes a transistor comprising:

a source region;

a drain region;

a channel region between the source and drain regions;

a floating gate separated from the channel region by an insulator; and

a control gate located adjacent to the floating gate and separated therefrom by an intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

39.(Amended)

The memory device of claim 32 wherein [the] an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than [the] an area of a capacitor formed by the floating gate, the insulator, and the channel region of each transistor.

Please add the following new claims:

4.(New)

The transistor of claim 19 wherein:

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

the floating gate comprises a material that has a smaller electron affinity than

polycrystalline silicon;

an area of a capacitor formed by the control electrode, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the barrier energy is less than approximately 2.0 eV.

42.(New) The memory cell of claim 29, further comprising:

a source region in a substrate;  
a drain region in the substrate;  
a channel region in the substrate between the source region and the drain region;  
an insulator between the storage electrode and the channel region, the insulator comprising a material that has a larger electron affinity than silicon dioxide, and a barrier energy between the insulator and the storage electrode being less than approximately 3.3 eV;

wherein the storage electrode comprises a material that has a smaller electron affinity than polycrystalline silicon; and

wherein an area of a capacitor formed by the control electrode, the storage electrode, and the intergate dielectric is larger than an area of a capacitor formed by the storage electrode, the insulator, and the channel region.

43.(New) A transistor comprising:

a source region in a substrate;  
a drain region in the substrate;  
a channel region in the substrate between the source region and the drain region;  
an insulator comprising a material that has a larger electron affinity than silicon dioxide;  
a floating gate separated from the channel region by the insulator, a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

a control gate, separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

44.(New) The transistor of claim 43 wherein:

the insulator comprises amorphous silicon carbide;  
the floating gate comprises a material that has a smaller electron affinity than polycrystalline silicon;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the barrier energy is less than approximately 2.0 eV.

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45.(New) A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

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a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon and a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

a control gate, separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

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46.(New) The transistor of claim 45 wherein:

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

the floating gate comprises polycrystalline or microcrystalline silicon carbide;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the barrier energy is less than approximately 2.0 eV.

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47.(New) A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV;

a control gate, separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and

wherein an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

48.(New) The transistor of claim 47 wherein:

the floating gate comprises a material that has a smaller electron affinity than polycrystalline silicon;

the insulator comprises a material that has a larger electron affinity than silicon dioxide; and

the barrier energy is less than approximately 2.0 eV.

49.(New) A transistor comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

an insulator comprising a material that has a larger electron affinity than silicon dioxide;

a floating gate separated from the channel region by the insulator; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

50.(New) The transistor of claim 49 wherein:

the insulator comprises amorphous silicon carbide;

a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;

the floating gate comprises a material that has a smaller electron affinity than polycrystalline silicon; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

51.(New) A transistor comprising:

- a source region in a substrate;
- a drain region in the substrate;
- a channel region in the substrate between the source region and the drain region;
- a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon; and
- a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

52.(New) The transistor of claim 51 wherein:

- a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;

- the floating gate comprises polycrystalline or microcrystalline silicon carbide;
- the insulator comprises a material that has a larger electron affinity than silicon dioxide;

and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

53.(New) A transistor comprising:

- a source region in a substrate;
- a drain region in the substrate;
- a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator;

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and

wherein an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

54.(New) The transistor of claim 53 wherein:

a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;

the insulator comprises a material that has a larger electron affinity than silicon dioxide; and

the floating gate comprises a material that has a smaller electron affinity than polycrystalline silicon.

55.(New) A memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

an insulator comprising a material that has a larger electron affinity than silicon dioxide;

a floating gate separated from the channel region by the insulator; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

56.(New) The memory cell of claim 55 wherein:

the insulator comprises amorphous silicon carbide;

a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;

the floating gate comprises a material that has a smaller electron affinity than polycrystalline silicon; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

57.(New) A memory cell comprising:

- a source region in a substrate;
- a drain region in the substrate;
- a channel region in the substrate between the source region and the drain region;
- a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon; and
- a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

58.(New) The memory cell of claim 57 wherein:

- the floating gate comprises polycrystalline or microcrystalline silicon carbide;
- a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;
- the insulator comprises a material that has a larger electron affinity than silicon dioxide;

and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

59.(New) A memory cell comprising:

- a source region in a substrate;
- a drain region in the substrate;
- a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator;  
a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and  
wherein an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

60.(New) The memory cell of claim 59 wherein:

a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;  
the insulator comprises a material that has a larger electron affinity than silicon dioxide;  
and  
the floating gate comprises a material that has a smaller electron affinity than polycrystalline silicon.

61.(New) A memory cell comprising:

a source region in a substrate;  
a drain region in the substrate;  
a channel region in the substrate between the source region and the drain region;  
a floating gate separated from the channel region by an insulator, a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and  
a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

62.(New) The memory cell of claim 61 wherein:

the barrier energy is less than approximately 2.0 eV;  
the insulator comprises a material that has a larger electron affinity than silicon dioxide;  
the floating gate comprises a material that has a smaller electron affinity than polycrystalline silicon; and



an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

63.(New) A memory device comprising:

a plurality of memory cells, each memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

an insulator comprising a material that has a larger electron affinity than silicon

dioxide;

a floating gate separated from the channel region by the insulator; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

64.(New) The memory device of claim 63 wherein:

the insulator comprises amorphous silicon carbide;

a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;

the floating gate comprises a material that has a smaller electron affinity than polycrystalline silicon;

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region; and

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

65.(New) A memory device comprising:

a plurality of memory cells, each memory cell comprising:

a source region in a substrate;

a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;

a floating gate separated from the channel region by an insulator, a barrier energy between the floating gate and the insulator being less than approximately 3.3 eV; and

a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

66.(New) The memory device of claim 65 wherein:

the barrier energy between the floating gate and the insulator is less than approximately 2.0 eV;

the insulator comprises a material that has a larger electron affinity than silicon dioxide;

the floating gate comprises a material that has a smaller electron affinity than polycrystalline silicon; and

an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

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67.(New) A memory device comprising:  
a plurality of memory cells, each memory cell comprising:  
a source region in a substrate;  
a drain region in the substrate;  
a channel region in the substrate between the source region and the drain region;  
a floating gate separated from the channel region by an insulator, the floating gate comprising a material that has a smaller electron affinity than polycrystalline silicon; and  
a control gate separated from the floating gate by an intergate dielectric, the intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide.

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68.(New) The memory device of claim 67 wherein:  
the floating gate comprises polycrystalline or microcrystalline silicon carbide;  
a barrier energy between the floating gate and the insulator is less than approximately 3.3 eV;  
the insulator comprises a material that has a larger electron affinity than silicon dioxide;  
an area of a capacitor formed by the control gate, the floating gate, and the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the insulator, and the channel region.

the memory device further comprises:  
a row decoder;  
a column decoder;  
a command and control circuit;  
a voltage control circuit; and  
wherein the memory cells are arranged in an array.

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69.(New) A memory device comprising:  
a plurality of memory cells, each memory cell comprising:  
a source region in a substrate;  
a drain region in the substrate;

a channel region in the substrate between the source region and the drain region;  
a floating gate separated from the channel region by an insulator;  
a control gate separated from the floating gate by an intergate dielectric, the  
intergate dielectric having a permittivity that is higher than a permittivity of silicon dioxide; and  
wherein an area of a capacitor formed by the control gate, the floating gate, and  
the intergate dielectric is larger than an area of a capacitor formed by the floating gate, the  
insulator, and the channel region.

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70.(New) The memory device of claim 69 wherein:

a barrier energy between the floating gate and the insulator is less than approximately 3.3  
eV;

the floating gate comprises a material that has a smaller electron affinity than  
polycrystalline silicon; and

the insulator comprises a material that has a larger electron affinity than silicon dioxide.  
the memory device further comprises:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.

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71.(New)

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The memory device of claim 37, further comprising:

a row decoder;

a column decoder;

a command and control circuit;

a voltage control circuit; and

wherein the memory cells are arranged in an array.